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Applications of Quasi-Floating-gate MOS Transistor in Universal Gates

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Abstract : The trend in integrated circuit fabrication since its inception has been a move towards decreasing geometry sizes in order to increase chip density, speed and reduce power consumption. The challenge of designing high performance low voltage and low power digital circuits is immense due to scaling down of CMOS technology and the increasing demand for portable electronic equipments. Low voltage and low power dissipation are important criteria for the design of sub-micron mixed mode circuits. There exist a number of design techniques for the design of low voltage analog and digital circuits. Amongst them, floating-gate MOSFET (FGMOS) has been widely used due to its unique characteristic of threshold voltage tunability through a bias voltage and its compatibility with CMOS technology. However, FGMOS suffers from low speed, large chip area besides a trapped offset charge at floating gate during fabrication. The use of quasi floating-gate MOSFET (QFGMOS) promises the removal of such limitations. This paper presents the design of universal gates using QFGMOS and it has been observed that the gates implemented with QFGMOS exhibit lower propagation delay and lower energy delay product vis-a-vis FGMOS and CMOS versions. Hence QFGMOS based logic gates would be more suitable in the realm of scaled down nanotechnology. The performance of these circuits has been verified through PSpice simulations carried out using level 7 parameters in 0.13 µm CMOS technology with a supply voltage of 1V.
Keywords:- Floating-gate MOSFET, Quasi Floating-gate MOSFET, Propagation delay, Energy delay product.

Introduction

The CMOS digital circuits with very low power consumption and high operating speed have always been the focus of the design criteria. Since there is always a trade-off between power dissipation and time delay in digital circuits, so reducing the power dissipation and still maintaining the high performance of circuits in terms of speed is important in digital designs. There is a need of new design techniques for optimum performance of devices to be operated at sub-volt supplies and consuming very low power with the continuous reduction of their dimensions. The power supply reduction is must with scaling down of devices but it happens at the expense of speed[1,2,3]. Since the performance of circuits can be altered with tuning of threshold voltage of transistors, therefore FGMOS has been abundantly employed to enhance the performance of mixed mode low voltage circuits despite their inherent limitations like reduced gain-bandwidth product and large chip area due to

the need of large biasing capacitance[4,5,6,7]. The use of Quasi-floating-gate MOSFET (QFGMOS) can further enhance the performance of circuits in terms of high speed and low power dissipation as compared to FGMOS. It is because of the fact that QFGMOS doesn't need a large biasing capacitance as its gate is feebly connected to supply voltage through a large value resistor[8,9].

Floating-Gate MOS transistor

Floating-Gate MOS transistor (FGMOS) is a modified form of simple MOSFET whose gate is floating and extra capacitances are introduced between the conventional gate and the multi-input signal gates as shown in Fig. 1. By applying a bias voltage on one of the input gates, the threshold voltage of FGMOS can be changed. Programming of the FGMOS introduces a charge on its floating-gate that shifts the threshold voltage and thus provides control over the device functionality[10].

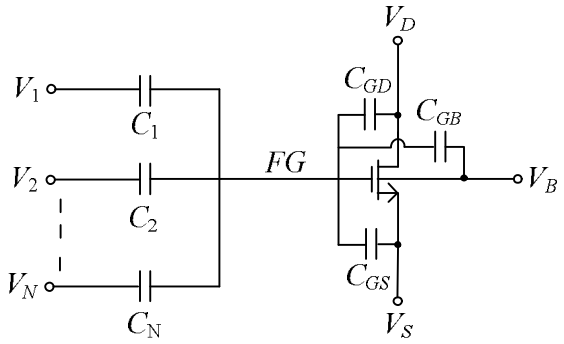

Fig. 1 Floating-gate MOSFET

Now, for 2- input FGMOS, the effective threshold voltage is given by[11]:

$$V_{T,eff} = \frac{(V_T - V_{bias}k_2)}{k_1} \quad (1)$$

where $k_1 = \frac{C_1}{C_T}$ and $k_2 = \frac{C_2}{C_T}$, C_1 and C_2 are the capacitances between floating-gate (FG) and control gates and $C_T = C_1 + C_2 + C_{GS} + C_{GD} + C_{GB}$. For reduction in effective threshold voltage from its conventional value V_T, C_2 has to be larger than C_1 for a positive V_{bias}. But the large coupling capacitance (C_2) makes silicon area large, resulting in reduction of effective transconductance and gain-bandwidth product. FGMOS circuits also have the problem of charge entrapment at FG during fabrication causing large dc offsets. These entrapped charges can no doubt be removed but it requires high supply voltage thus defeating the concept of low voltage design[12]

These limitations can be further overcome by quasi-floating-gate MOSFET (QFGMOS) as depicted in Fig. 2 where gate is not floating like FGMOS but is weakly connected to one of the supply rails through a high value resistor[13]. Here, the gate is not left floating for dc, instead a large valued resistor implemented through a reverse biased MOSFET is attached to the gate of the transistor and then appropriately connected to one of the power supplies[14].

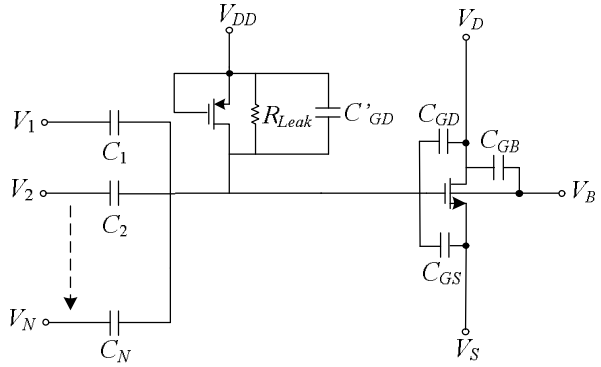

Fig. 2 Quasi-floating-gate MOSFET

The effective threshold voltage of QFGMOS is given by:

$$V_{T,eff} = \frac{(V_T - V_{DD}k_2)}{k_1} \quad (2)$$

where $k_1 = \frac{C_1}{C_T}$ and $k_2 = \frac{C'_{GD}}{C_T}$ and $C_T = C_1 + C'_{GD} + C_{GS} + C_{GD} + C_{GB}$

NAND gate using FGMOS

The performance of NAND gate can be ascertained through its transient or dynamic response to obtain propagation delay which determines the maximum operating speed of the device and is defined as[15]:

$$t_p = \frac{(t_{PLH} + t_{PHL})}{2} \quad (3)$$

where t_{PLH} defines the response time of the gate for a low to high output transition, while t_{PHL} refers to the response time for high to low output transition. Further propagation delay of simple CMOS NAND gate can be expressed as[16]:

$$t_p = 0.35C_L\left[\left(\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{DD} - V_{Tn})\right)\left(\mu_p C_{ox}\left(\frac{W}{L}\right)_p (V_{DD} - V_{Tp})\right)\right]^{-1} \quad (4)$$

Since t_p depends on threshold voltage of N-channel and P-channel MOSFETs, therefore it is expected that it can be optimized using FGMOS where threshold voltage tunability is feasible. The circuit topology of FGMOS NAND gate as shown in Fig. 3 is similar to CMOS NAND gate [16]. The bias voltages V_{bp} and V_{bn} provide tunability to the threshold voltages of P-channel and N-channel FGMOS transistors respectively and hence characteristics of the NAND gate can be improved.

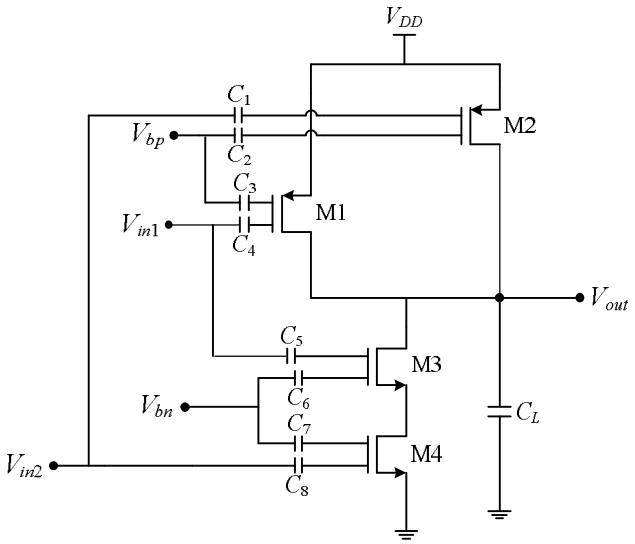

Fig. 3 NAND gate using FGMOS

Now, the propagation delay for FGMOS NAND gate is given by:

$$t_p = 0.35C_L\left[\beta_n\left(V_{DD} - \frac{(V_{Tn} - V_{bn}k_2)}{k_1}\right)\beta_p\left(V_{DD} - \frac{(V_{Tp} - V_{bp}k_2)}{k_1}\right)\right]^{-1} \quad (5)$$

Thus propagation delay can be reduced and speed can be enhanced when conventional MOSFETs in NAND gate are replaced by FGMOS. The circuit of FGMOS NAND gate is simulated for the transient response at different values of V_{bp} and V_{bn} by selecting W/L of M1 and M2 as 2.6 µm/0.13 µm and M3 and M4 as 1.3 µm/0.13 µm with the supply voltage of 1 V and is shown in Figs. 4 and 5 respectively. In Fig. 4, bias voltage of P-channel FGMOS (V_{bp}) is varied from 0 V to 1 V, while keeping bias voltage of N-channel FGMOS (V_{bn}) fixed at 1 V. Similarly in Fig. 5, V_{bn} is varied from 0 V to 1 V, while keeping V_{bp} fixed at 0 V and output voltage (V_{out})

is obtained with respect to time. It has been observed that transient response in FGMOS NAND gate can be varied with bias voltage resulting in different values of propagation delay.

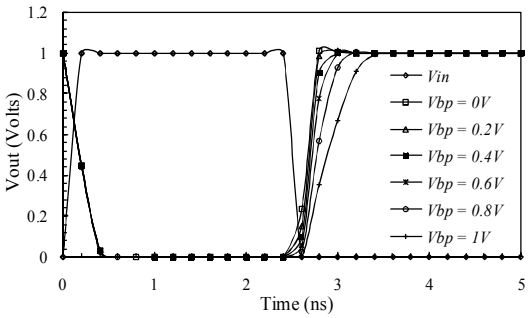

Fig. 4 Transient response of FGMOS NAND gate at different V_{bp}

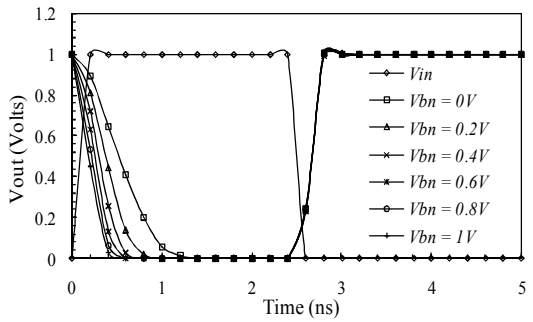

Fig. 5 Transient response of FGMOS NAND gate at different V_{bn}

Now, the variation of propagation delay as a function of bias voltages is shown in Fig. 6 which shows that as we increase the bias voltage of P-channel FGMOS from 0 V to 1 V, delay increases from 0.18 ns to 0.42 ns, where as increasing bias voltage of N-channel FGMOS reduces time delay from 0.50 ns to 0.18 ns. Therefore propagation delay and hence the speed of FGMOS based NAND gate can be optimized by suitably adjusting the bias voltages of N and P-channel FGMOS.

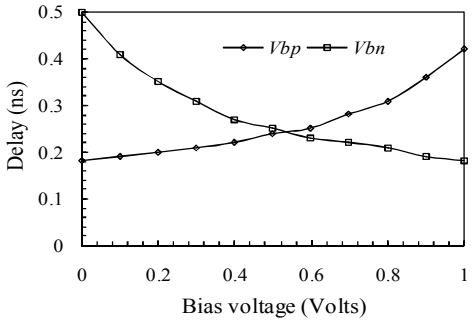

Fig. 6 Variation of delay with bias voltage

NAND Gate using QFGMOS

Since the limitations of FGMOS can be overcome by QFGMOS, so the NAND gate based on QFGMOS will exhibit better performance than its FGMOS counterpart. The circuit of NAND gate using QFGMOS is shown in Fig. 7.

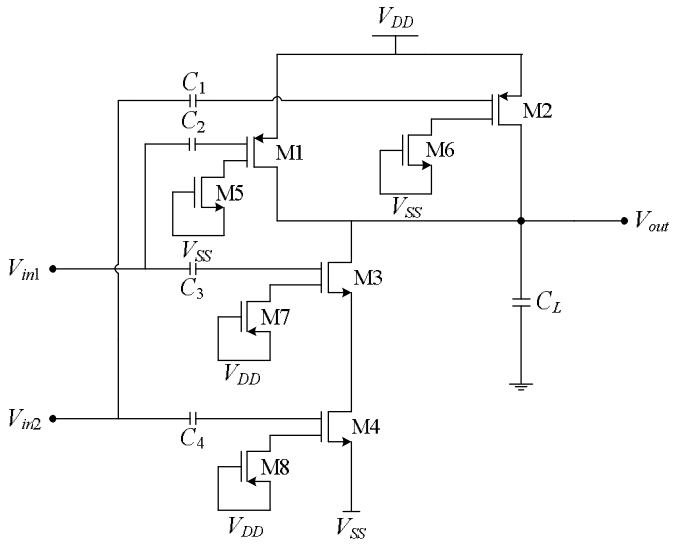

Fig. 7 NAND gate using QFGMOS

Now, the propagation delay for QFGMOS NAND gate is given by:

$$t_p = 0.35C_L\left[\beta_n\left(V_{DD} - \frac{(V_{Tn} - V_{DD}k_2)}{k_1}\right)\beta_p\left(V_{DD} - \frac{(V_{Tp} - V_{SS}k_2)}{k_1}\right)\right]^{-1} \quad (6)$$

Since k_2 in QFGMOS is smaller than that of FGMOS as $C'_{GD} << C_2$, the total effective capacitance C_T is less than that of FGMOS and hence propagation delay of QFGMOS will also be reduced[17].

Now, the comparative transient characteristics of NAND gate using CMOS, FGMOS and QFGMOS have been obtained by selecting same *W/L* of M1, M2, M7 and M8 as 2.6 µm/0.13 µm and M3, M4, M5 and M6 as 1.3 µm/0.13 µm while keeping bias voltages of P-channel and N-channel FGMOS transistors fixed i.e. V_{bp} = 0 V and V_{bn} = 1 V with a supply voltage of 1 V and are shown in Fig. 8.

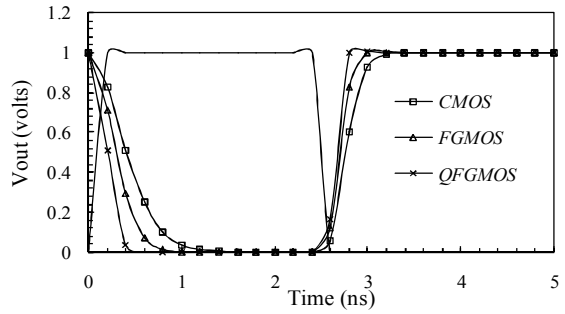

Fig. 8 Comparative transient response of NAND gate

It has been observed that NAND gate using QFGMOS has propagation delay of 0.11 ns which is less as compared to FGMOS (0.18 ns) and CMOS NAND gate (0.28 ns).

Now, the values of propagation delay obtained from the transient analysis of NAND gate using CMOS, FGMOS and QFGMOS has been used to calculate the energy delay product (EDP) at different values of supply voltage V_{DD}. The comparative EDPs of NAND gate using CMOS, FGMOS and QFGMOS are shown in Fig. 9.

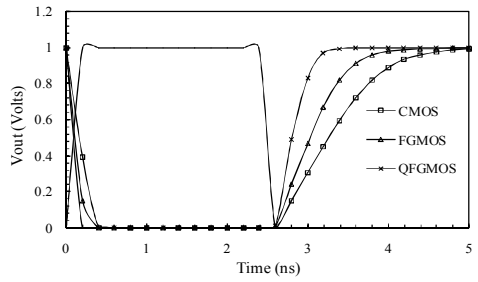

Fig. 9 Comparative EDPs of NAND gate

In Fig. 9, we find that EDP depends on V_{DD} and for V_{DD} of 1V, EDP of QFGMOS based NAND gate is 0.55E-23 Js where as the values of EDP for FGMOS and CMOS based NAND gate are 0.9E-23 Js and 1.4E-23 Js respectively. Thus, QFGMOS based NAND gate shows better performance and can be operated at low voltage.

NOR Gate using QFGMOS

Similarly, the performance of CMOS NOR gate can be improved when conventional MOSFETs are replaced by QFGMOS as shown in Fig. 10.

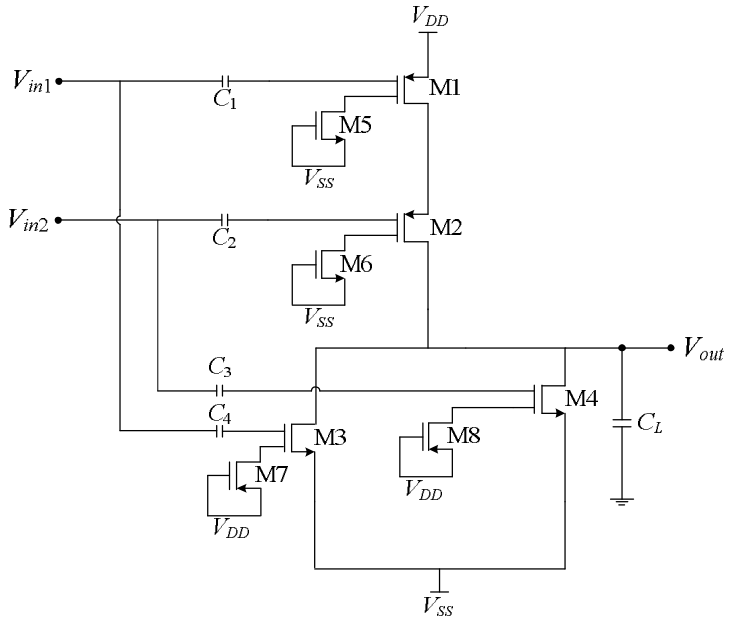

Fig. 10 NOR gate using QFGMOS

The comparative transient characteristics of NOR gate using CMOS, FGMOS and QFGMOS have been obtained by selecting same *W/L* of M1, M2, M7 and M8 as 2.6 µm/0.13 µm and M3, M4, M5 and M6 as 1.3 µm/0.13 µm while keeping bias voltages of P-channel and N-channel FGMOS fixed i.e. V_{bp} = 0 V and V_{bn} = 1 V with supply voltage of 1 V and are shown in Fig. 11. It has been found that NOR gate using QFGMOS has propagation delay of 0.15 ns which is less as compared to FGMOS (0.24 ns) and CMOS NOR gate (0.42 ns).

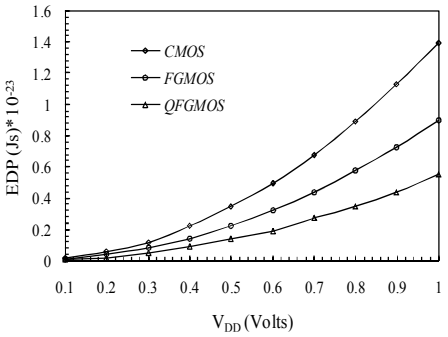

Fig. 11 Comparative transient response of NOR gate

Again, the values of propagation delay obtained from the comparative transient responses of NOR gate has been used to calculate the energy delay product (EDP) at different values of supply voltage V_{DD}. The comparative EDPs of NOR gate are shown in Fig. 12.

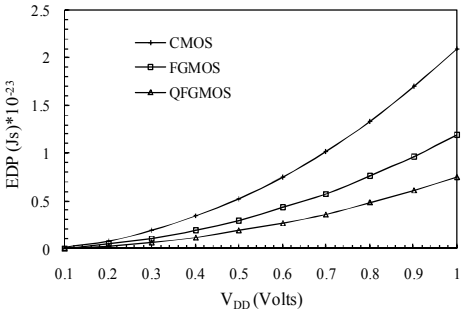

Fig. 12 Comparative EDPs of NOR gate

It has been observed in Fig. 12 that EDP of QFGMOS based NOR gate is minimum (0.75E-23 Js) at V_{DD} = 1V, while it is 1.2E-23 Js for FGMOS and 2.1E-23 Js for CMOS, implying better performance of QFGMOS NOR gate at low supply voltages. The performance comparison of NAND and NOR gates using CMOS, FGMOS and QFGMOS at supply voltage of 1 V is presented in Table 1.

Table 1 Performance comparison of NAND and NOR gates

Devices	Parameters	Propagation delay (t_p)	Energy delay product (*EDP*)
NAND Gate	CMOS	0.28 ns	1.4 E-23 Js
	FGMOS	0.18 ns	0.9 E-23 Js
	QFGMOS	0.11 ns	0.55 E-23 Js
NOR Gate	CMOS	0.42 ns	2.1 E-23 Js
	FGMOS	0.24 ns	1.2 E-23 Js
	QFGMOS	0.15 ns	0.75E-23 Js

Conclusions

In this paper, we have discussed the technique of improving the characteristics of NAND and NOR gates through variation of bias voltage. We have also designed these gates using FGMOS and QFGMOS. It has been observed that propagation delay and energy delay product of QFGMOS based digital gates is less as compared to their FGMOS and CMOS versions. Therefore, QFGMOS can be used as an alternate technique for the design of low voltage digital circuits where high speed and low power dissipation are the primary concerns. The performance of these circuits has been verified through PSpice simulations carried out using level 7 parameters in 0.13 µm CMOS technology with a supply voltage of 1V.

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